CLAIMS

We claim:

1. A managing system for managing a plurality of VRMs associated with a plurality of microprocessors and connected in parallel together between first and second voltage references, said VRMs having output terminals connected together and arranged to communicate over a common bus, wherein said managing system comprises:

an error amplifier (3) being input an output voltage signal from said plurality of VRMs, a reference voltage, and a droop voltage produced through an equivalent droop resistor receiving an output current signal (Iout) from said plurality of VRMs and being connected to said common bus, said error amplifier effecting a comparison of said input signals to generate a control voltage signal to said plurality of VRMs; and

a controller connected to said equivalent droop resistor.

2. A managing system according to claim 1, comprising:

at least a first summing node, being connected to said error amplifier and said equivalent droop resistor and arranged to output a control voltage signal to said plurality of VRMs, said first summing node receiving a reference voltage as a positive addend and receiving, as negative addends, a droop voltage and a total voltage resulting from a summation, performed in a second summing node, of an output voltage signal from said plurality of VRMs, said second supply voltage reference;

first and second control resistors connected, in series with each other, to said common bus to receive said output current signal; and

a third summing node, being input a first local control voltage from said first control resistor as a positive addend and a second local control voltage from said second control resistor as a negative addend;

wherein said controller is connected to an input of said third summing node and supplies an internal control voltage directly to said equivalent droop resistor.

3. A managing system according to Claim 2, wherein said error amplifier comprises an operational amplifier having a first input terminal to receive said reference voltage and an output terminal feedback-connected, through a capacitor, to a second input terminal thereof, said second input terminal being connected to an internal circuit node, said internal circuit node receiving the sum of a droop current, an internal control current, and said output voltage signal from the VRM plurality through a feedback resistor passing said sum of currents.

4. A managing system according to Claim 3, wherein said internal circuit node is connected to a compensating sub-system, said compensating sub-system comprising a compensation resistor to receive the sum of said control voltage and said reference voltage.

5. A managing system according to Claim 4, wherein a regulated voltage signal is output being equal to:

$$Vref - Idroop*Rfb - Vshare*Rfb/Rc,$$

said droop current being proportional to the value of said output current signal from the VRM plurality, and said control voltage being proportional to the ratio Iload/N-Iout, where N is the number of cascaded modules in said VRM plurality.

6. A method of synchronizing a plurality of VRMs associated with a plurality of microprocessors and connected in parallel together between first and second voltage references, said VRMs having output terminals connected in parallel to a common bus line, the method comprising the following steps:

in an initial turn-on situation, said bus line is pulled up by raising a voltage on said bus line above a high tripping threshold; and

detecting an overload or an overvoltage condition, wherein a VRM that has detected the condition transmits an indication of such detecting to the other VRMs connected in parallel to the bus line, thereby pulling down said bus line by pulling the voltage on said bus line below a low tripping threshold.

7. A synchronizing method according to Claim 6, wherein:

when the overload condition or a short-circuit condition is followed by a re-initialization procedure, the VRM that detected the overload or the short-circuit condition releases the bus line to normal operation above said low tripping threshold and below said high tripping threshold; and

said re-initializing procedure is followed by a turn-on procedure.

8. A synchronizing method according to Claim 7, wherein, after a set number of re-initialization procedures are completed because of either an overload or a short-circuit condition, said VRM that detected the overload or the short-circuit condition holds the bus line at a value equal to said second supply reference until the supply references are pulled down and then up and an indication of a faulty condition is issued.

9. A synchronizing method according to Claim 6, wherein each VRM includes an internal line and, in the initial turn-on situation:

each VRM pulls its respective internal line high that corresponds to a first local control voltage before entering the turn-on situation;

with the voltage on said bus line being the mean of the local control voltages of the VRMs, the bus line only goes high when all the VRMsare ready to enter the turn-on situation; and

at this point, all said VRMs enter the turn-on situation simultaneously when said VRMs drop the respective internal lines of the local control voltage, allowing a current sharing loop to operate as normal on a voltage lying between said low tripping threshold and said high tripping threshold.

10. A synchronizing method according to Claim 6, wherein, under the overload, a short-circuit, or the overvoltage condition, said bus voltage is pulled to the same value as said second supply reference.

11. A synchronizing method according to Claim 6, wherein, under the overvoltage condition, said VRM that detected the overvoltage condition only releases said bus line after the supply references are pulled down and then up and said VRMs enter a turn-on phase.

12. A synchronization circuit integrated in a VRM of a plurality of VRMs cascade-connected to a common bus that includes a common bus line, comprising:

a high comparator connected to said common busline, the high comparator having a high tripping threshold and being structured to monitor a bus voltage on said common bus line and, in response to detecting an overload or an overvoltage condition, transmit an indication of such detecting to the other VRMs connected in parallel to the common bus, thereby pulling down said bus line by pulling the voltage on said bus line below a low tripping threshold; and

a low comparator connected to said common bus and structured to monitor the bus voltage on said common bus line and detect when the bus voltage drops below the low tripping threshold.

13. A control system for controlling a first voltage reference module that outputs an output voltage, comprising:

a first error amplifier having a first inputs and an output, the first input being coupled to the output;

a feedback resistor coupled between the output voltage and the first input of the first error amplifier;

a first current generator coupled to the first input of the first error amplifier; and

a controller having second current generator coupled to the first input of the error amplifier, the second current generator being responsive to a voltage on a common bus connected between the first voltage reference module and a second voltage reference module.

14. A control system according to claim 13 wherein the first error amplifier further comprises a second input coupled to a voltage reference.

15. A control system according to claim 14, further comprising a second error amplifier having a first input coupled to the common bus, a second input coupled to one of the inputs of the first error amplifier, and an output coupled to the second current generator.